IN THE CLAIMS

1. (Canceled).

2. (Currently Amended) [[The]] A nonvolatile data storage circuit ~~according to Claim 1~~, comprising:

a data holding circuit having a storage node; and

a plurality of ferroelectric capacitors one electrode of each of which is connected to said storage node; wherein

during a store operation to write data from said data holding circuit to said plurality of ferroelectric capacitors, a plurality of plate signals are supplied to the other electrodes of said plurality of ferroelectric capacitors, timing of either rising or falling, or of both the rising and falling of the plurality of plate signals being made different, and

wherein said data holding circuit comprises a latch circuit in which input and output terminals of a pair of inverters are cross-connected, and said storage node is the pair of input and output terminals.

3. (Currently Amended) The nonvolatile data storage circuit according to Claim [[1]] 2, wherein the plurality of ferroelectric capacitors connected to said storage node have a first and a second ferroelectric capacitor, and the timing of the falling of a first plate signal and the timing of the rising of a second plate signal, applied to said first and second ferroelectric capacitors, substantially coincide.

4. (Original) The nonvolatile data storage circuit according to Claim 3, wherein said data holding circuit comprises an activation circuit which activates the data holding circuit in response to an activation signal; and, during a recall operation to write data

from said ferroelectric capacitors to said data holding circuit, after said first plate signal has been driven, said data holding circuit is activated by said activation circuit.

5. (Original) The nonvolatile data storage circuit according to Claim 4, wherein during said recall operation, after activation of said data holding circuit, said second plate signal is driven to write data to said ferroelectric capacitors.

6. (Original) The nonvolatile data storage circuit according to Claim 4, wherein during said store operation and said recall operation, said first and second plate signals have the same timing waveforms.

7. (Original) A nonvolatile data storage circuit, comprising:

a data latch circuit having first and second storage nodes;

first and second ferroelectric capacitors one electrode of which is connected to said first storage node, and third and fourth ferroelectric capacitors one electrode of which is connected to said second storage node; wherein

during a store operation to write data of said data latch circuit to said ferroelectric capacitors, a first plate signal is supplied to the other electrodes of said first and third ferroelectric capacitors, a second plate signal is supplied to the other electrodes of said second and fourth ferroelectric capacitors, and the timing of either the rising or the falling, or both, of said first and second plate signals are made different.

8. (Original) The nonvolatile data storage circuit according to Claim 7, wherein during said store operation, the timing of the falling of said first plate signal and the rising of said second plate signal substantially coincide.

9. (Original) The nonvolatile data storage circuit according to Claim 7, wherein during the recall operation to write the data from said ferroelectric capacitors to the data latch circuit, said first plate signal is supplied to the other electrodes of said first and third ferroelectric capacitors, then said data latch circuit is activated, and thereafter, said second plate signal is supplied to the other electrodes of said second and fourth ferroelectric capacitors.

10. (Original) The nonvolatile data storage circuit according to Claim 7, wherein a dummy gate circuit is connected to either said first storage node or to said second storage node to equalize the parasitic capacitances.

11. (Original) The nonvolatile data storage circuit according to Claim 7, wherein said data latch circuit has a pair of inverters with input and output terminals cross-connected, and the pair of inverters have a p-channel transistor and an n-channel transistor, having substantially same current driving abilities.

12. (Original) A nonvolatile data storage circuit, comprising:

a data holding circuit having a storage node; and

a pair of ferroelectric capacitors one electrode of each of which is connected to said storage node; wherein

during a recall operation to rewrite data from said ferroelectric capacitors to said data holding circuit, the timing of first and second plate signals supplied to the other electrodes of said pair of ferroelectric capacitors is shifted, when said first plate signal is applied said data holding circuit is activated to latch the data, and thereafter said second plate signal is applied.

13. (Original) A nonvolatile memory circuit, comprising:

a plurality of word lines;

a plurality of bit line pairs; and

a plurality of memory cells placed at positions of intersection of said word lines and said bit line pairs; wherein

each of said memory cells has a data latch circuit having first and second storage nodes, first and second ferroelectric capacitors one electrode of each of which is connected to said first storage node, and third and fourth ferroelectric capacitors one electrode of each of which is connected to said second storage node; and,

during a store operation to write data from said data latch circuit to said ferroelectric capacitors, a first plate signal is supplied to the other electrodes of said first and third ferroelectric capacitors, a second plate signal is supplied to the other electrodes of said second and fourth ferroelectric capacitors, and timing of either rising or falling, or both, of said first and second plate signals is different.

14. (Original) The nonvolatile memory circuit according to Claim 13, wherein during said store operation, the timing of the falling of said first plate signal and of the rising of said second plate signal substantially coincide.

15. (Original) The nonvolatile memory circuit according to Claim 13, wherein during a recall operation to write the data from said ferroelectric capacitors to the data latch circuit, said first plate signal is supplied to the other electrodes of said first and third ferroelectric capacitors, then said data latch circuit is activated, and thereafter, said

second plate signal is supplied to the other electrodes of said second and fourth ferroelectric capacitors.